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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,616	12/19/2000	Lizy Kurian John	119927-1040	5809

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,616	JOHN ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/08/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-38 are presented for examination.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1,2,8-10,12-21,23-27,31,35-37,38 are rejected under 35 U.S.C. 102(a)(b) as being anticipated by Nakagawa et al. (5,651,123)

4. As to claim 1, 38, the claimed language :'resources within a processor " (claim 1) is interpreted as any processing source in a data processing system, such as instructions stored in specific memory addresses based on applicant's own disclosure (see page 3, lines 11-20). No specfic structure of the "processor" (claims 1, and 38) has been reflected into the claim, therefore, the "processor" is read as any type of processing sysytem. Applicant is welcome to give feedback in the next response. Nakagawa disclosed a system including at least :

a) a sequence generator that generate one or more resource identifiers [ID] using at least portion of the pseudo sequence within a processor (e.g. see col.8, lines 38-67, col.9, lines 1-11, see also fig.8 for the corresponding index O7-O0);

b)resource identifier selector [selector] coupled to the sequence generator (e.g. see figs.3,5,15 see also col.7, lines 26-67, col.8, lines 1-5) for selecting one or more resource id for instruction allocation.

5. Nakagawa taught a generation of resource identifiers corresponding to a processor resource [memory location] (e.g. see col.7, lines 25-29). Nakagawa generated program was directed to addresses corresponding to locations in an instruction memory. The locations in the instruction memory are processor resources because instructions are being used by the processor.

6. See also Nakagawa's fig.3 , random generator, which included plurality of selectors for selecting an identifier [address of an instruction] in , col.7, lines 25-29) from one or more identifiers (see a series of random numbers by the selectors in col.7, lines 33-58) allocated to the instruction (i.e. outputting of instruction address for a given instruction).

7. Nakagawa also included at least :

a) memory storage device (e.g. see fig.4 [Memory]);

b)a bus (fig.4 [36]);

c) a processor [30] coupled to the bus comprising a resource allocator (see fig.4).

8. As to claim 2, Nakagawa also determined how many id's needed (e.g. see the number sequence of 126 in col.8, lines 1-12).

9. As to claims 8-10, Nakagawa disclosed logic circuit (fig.5 [selection]) and storage array (see fig.5 [register]).

10. As to claim 12, Nakagawa was also directed to pseudorandom sequence (e.g. see col.3, lines 35-36).

11. As to claim 13, Nakagawa also generated a pseudorandom number based on a first pseudo number (e.g. see the sequential generation of he random numbers in fig.8).

12. As to claims 14, 17, 23,35-37, Nakagawa also stored the random number as elements in a storage array (e.g. see each value of the random number in respective register in fig.5, see also the selector for the logic circuit and the register array for the storage array).

13. As to claims 15, 18,24, Nakagawa also included least significant bit (e.g. see fig.8 O0 bit in the table).

14. As to claims 16,25, Nakagawa also included a shifter (e.g. see the feedback shift register in col.4, lines 13-24) and the selection circuit for indexing the element of the array (e.g. see the selection of the output address in col.7, lines 25-67, col.8, lines 1-5).

15. As to claim 19, Nakagawa also determined the highest identifier (e.g. see the 1-126 range in col.8, lines 1-12).

16. As to claim 21, Nakagawa also determined how many identifiers required (e.g. see, col.2, lines 29-41, col.8, lines 1-8).

17. As to claim 26, Nakagawa also included determining a number based the most recent associated identifier (e.g. see the fixed sequence of the random numbers in col.1-6).

18. As to claim 27, Nakagawa's identifier was also associated with instruction (e.g. see col.9, lines 12-22, see the random number of each instruction in figs.8-12).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 3 ,4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa et al. (5,651,123) in view of Gupta et al. (5,490,280).

20. As to claims 3,4, Gupta did not disclose the reorder buffer the buffer entries and as claimed. However, Gupta disclosed a reorder buffer and buffer entries (e.g. see fig.,1B, fig.2). It would have been obvious to one of ordinary skill in the art to use Gupta

in Nakagawa for including the reorder buffer and the buffer entries as claimed because the use of Gupta could provide the control capability of Nakagawa to easily allocate the resource information (e.g. id, data etc.) in a predetermined , thereby providing operand data requested at specific order of the instruction execution sequence from a single set of buffer entries, and therefore, reducing the latency cycle caused by separate hardware circuit, and it could be readily done by predefining the reorder buffer of Gupta into Nakagawa with modified configuration parameters (e.g. the buffer R/W port), such that the reorder buffer of Gupta could be recognized by Nakagawa, and one of ordinary skill in the art should be able to recognize that the locking mechanism of Nakagawa's arbitration among the plurality of peripheral devices would have needed a storage buffer, such as reorder buffer , for providing specific operation order of the resources to enhance the arbitration, and in doing so, provided a motivation.

21. Claims 5,6,7,22,28, 29, 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa et al. (5,651,123) in view of Williams et al. (5,530,837).

22. As to claims 5,6,7,22, 28,29, 32-34, limitations of the parent clams have been discussed in the previous paragraph, therefore, they are not repeated herein. Nakagawa did not specifically show his selector comprised the comparator for comparing the ID to an allocation bound as claimed. However, Williams discloses system for including a comparison of allocation bound (range) (see the bank id and the range comparison (e.g. see col.5, lines 56-65, col.6, lines 6-22). It would have been obvious to one of ordinary skill in the art to use Williams in Nakagawa for including the comparator for comparing the resource id with the allocation bound as claimed

because the use of Williams could provide Nakagawa the processing ability to allocate the id into a predetermined range of the resource identification , and therefore, eliminating possible contentions of the resource assignment by providing the comparison of he given range, and because it would have been obvious to one or ordinary skill in the art to recognize that allocation of the resource id within a defined group of allocation range or bound seemed to be logical and desirable in order to minimize the conflicts among the resource id's, otherwise, the system could not worked in efficient manner, and for the above reasons provided motivation .

23. Claims 11, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable Nakagawa et al. (5,651,123) in view of Kondo et al. (6,389,562).

24. As to claims 11, 30, Nakagawa did not specifically teach the stall signal for the decoder as claimed. However, Kondo disclosed a system including a stall signal for a decoder (e.g. see col.14, lines 5-10). It would have been obvious to one of ordinary skill in the art to use Kondo in Nakagawa for including the decoder stall signal as claimed because the use of Kondo could provide the processing capability of Nakagawa to adapt to particular processing condition of the circuit , such as the delay time due to error, therefore, increasing the accuracy of the corresponding processing sequence, such as the decode stage, at a given clock cycle, and it could be readily achieved by configuring the stall signal of Condo into Nakagawa so the decode stall signal could be recognized by Nakagawa.

25. Nakagawa et al. (5,651,123) , Gupta et al. (5,490,280), Williams et al. (5,530,837), Kondo et al. (6,389,562) have been cited to applicant in a previous action, therefore, copies of these patents are not provided herein.

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Togawa (6,038,585) is cited for the teaching of an instrucioin resource id (see the instrucion book ID in col.5, lines 1-67).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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21 Century Strategic Plan

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